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EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 07/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,598	HAMMARLUND ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 25-29* is/are rejected.

7)☒ Claim(s) *20-24 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been examined.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

3. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

4. The title of the invention is not descriptive. It is not clear what "stick and spoke replay" is and how it is related to the claimed invention. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The disclosure is objected to because of the following informalities: The specification contains no summary section. See below.

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data shet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic

documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000. Or alternatively, Reference to a "Microfiche Appendix": See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.

(e) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(f) **Brief Summary of the Invention**: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(g) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(h) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(i) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(j) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(k) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

6. Appropriate correction is required.

Claim Objections

7. Claims 2, 11, 15, 21, 23 and 29 are objected to because of the following informalities:

a. Claim 2 recites the limitation, "if a slot comes available" on its second and third lines. Please correct the claim language to more clearly read, "if a slot becomes available".

b. Claim 11 recites the limitation, "if a time slot become available" on its second line. Please correct the claim language to more clearly read, "if a time slot becomes available".

c. Claim 15 recites the limitations, "comprising tracking number of times" on its first line and "increased as number of times" on its third line. Please correct the

claim language to more clearly read, "comprising tracking **the** number of times" and "increased as **the** number of times", respectively.

d. Claim 21 recites the limitation, "coupled to said execution" on its sixth line. Please correct the claim language to more clearly read, "coupled to said execution unit".

e. Claim 23 recites the limitations, "memory hierarchy comprises of said first level cache" on its fourth line and "has fastest access time and disk memory has longest access time" on its fifth and sixth lines. Please correct the claim language to more clearly read, "memory hierarchy **is comprised** of said first level cache" and "has **the** fastest access time and disk memory has **the** longest access time", respectively.

f. Claim 29 recites the limitation, "to retire each instruction receive from said checker" on its second line. Please correct the claim language to more clearly read, "to retire each instruction **received** from said checker".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 2-8 and 10-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Claim 2 recites the limitation, "wherein said routing said instruction comprises advancing said instruction forward for replay into an earlier replay time slot if a slot comes available". However, the parent claim of claim 2, claim 1, recites "routing said instruction for immediate re-execution". It is unclear how an instruction that is being routed for immediate re-execution can be moved forward into an earlier replay slot, when if it is being re-executed immediately there are no replay slots. Please correct the claim language to more clearly define the metes and bounds of the claimed invention. Dependent claims 3-8 are rejected for the same reasons as above, as they contain all of the limitations of their parent claims.

11. Claim 10 recites the limitation, "determining whether a long latency type of error caused said instruction to execute incorrectly if said instruction did not execute incorrectly". It is unclear how it can be determined what type of error caused an instruction to execute incorrectly if it executed correctly (did not execute **in**correctly). Please correct the claim language to more clearly define the metes and bounds of the claimed invention. Dependent claims 11-16 are rejected for the same reasons as above, as they contain all of the limitations of their parent claims.

12. Claim 11 recites the limitation, "shifting said instruction forward for earlier replay if a time slot becomes available and shifting said instruction backwards for later replay if a resource conflict is detected". It is unclear what this "shifting" is performed on and what the actual "shift" comprises, as it could be comprised in an instruction queue, simply a logical shift, or something else all together. Please correct the claim language to more clearly define the metes and bounds of the claimed invention. Dependent claims 12-16 are rejected for the same reasons as above, as they contain all of the limitations of their parent claims.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 1-4, 9-14, 17-18 and 25-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Keller et al., U.S. Patent No. 6,622,235.

15. Regarding claim 1, Keller has taught a method comprising:

a. Dispatching an instruction for execution (see Col.8 line 51 – Col.9 line 3 and Col.12 lines 24-26),

b. Speculatively executing said instruction (see Col.12 lines 59-67, Col.19 lines 8-34 and Col.35 lines 16-31),

c. Determining whether said instruction executed correctly (see Col.2 lines 58-66 and Col.15 lines 7-12),

d. Routing said instruction to a replay mechanism if said instruction did not execute correctly (see Col.2 lines 58-66),

e. Determining whether incorrect executing of said instruction is due to a long latency operation (see Col.3 lines 8-19 and Col.15 lines 7-32),

f. Routing said instruction for immediate re-execution if said incorrect execution is not due to said long latency operation (see Col.3 lines 8-19 and Col.31 lines 8-29),

g. Delaying routing of said instruction for re-execution if said incorrect execution is due to said long latency operation (see Col.3 lines 8-19 and Col.15 lines 33-42),

h. Re-executing said instruction if said instruction did not execute correctly (see Col.2 lines 58-66 and Col.3 lines 8-19),

i. Retiring said instruction if said instruction executed correctly (see Col.11 lines 32-39).

16. Regarding claim 2, Keller has taught the method of claim 1, wherein said routing said instruction comprises advancing said instruction forward for replay into an earlier replay time slot if a slot comes available (see Col.18 lines 1-26). Here, the issue pick circuit selects the oldest eligible instructions from the ROP buffer every clock cycle to be issued/reissued for execution. Because instructions that are to be replayed reside within the ROP buffer, and because the oldest eligible instructions are issued first, every time an instruction is issued out of the buffer, inherently every other instruction is "moved forward" to an earlier time slot in the buffer.

17. Regarding claim 3, Keller has taught the method of claim 2, wherein said delaying routing of said instruction comprises moving said instruction backwards in time as resource conflicts are detected (see Col.18 lines 1-26). Here, the issue pick circuit selects the oldest eligible instructions from the ROP buffer every clock cycle to be issued/reissued for execution. Because instructions that are to be replayed reside within the ROP buffer, and because

instructions are ineligible for reissuing until their resource conflicts are resolved (see Col.15 lines 33-42), instructions that are to be replayed but still have pending resource conflicts (ineligible instructions) are inherently "moved backwards" into a later time slot in the buffer as they are passed over as younger, eligible instructions are issued.

18. Regarding claim 4, Keller has taught the method of claim 3, further comprising:

a. Routing said instruction to a delay queue (80 of Fig.4) to wait a period of time before re-executing said instruction if said incorrect execution is due to said long latency operation (see Col.15 lines 33-42, Col.17 lines 13-18, Col.18 lines 1-26 and Col.18 line 62 – Col.19 line 7),

b. Determining what type of error caused said instruction to execute incorrectly (see Col.15 lines 7-64),

c. Predicting what length time period to delay said instruction prior to routing said instruction for re-execution if said incorrect execution is due to said long latency operation (see Col.15 lines 33-42, Col.17 lines 13-18, Col.18 lines 1-26 and Col.18 line 62 – Col.19 line 7). Here, because the instruction is not allowed to be rescheduled for execution until an event occurs, the length of delay until the event occurs has been "predicted" prior to the event actually occurring.

19. Regarding claim 9, Keller has taught a method, comprising:

a. Dispatching an instruction (see Col.8 line 51 – Col.9 line 3 and Col.12 lines 24-26),

b. Speculatively executing said instruction (see Col.12 lines 59-67, Col.19 lines 8-34 and Col.35 lines 16-31),

c. Checking whether said instruction executing correctly (see Col.2 lines 58-66 and Col.15 lines 7-12),

d. Replaying said instruction if said instruction did not execute correctly (see Col.2 lines 58-66 and Col.3 lines 8-19), wherein said replaying comprises dynamically determining a time period to delay said instruction prior to re-execution (see Col.15 lines 33-42 and Col.18 line 62 – Col.19 line 7),

e. Re-executing said instruction after said time period elapsed if said instruction did not execute correctly (see Col.3 lines 8-19 and Col.15 lines 33-42),

f. Retiring said instruction if said instruction executed correctly (see Col.11 lines 32-39).

20. Regarding claim 10, Keller has taught the method of claim 9, wherein said checking further comprises determining whether a long latency type of error caused said instruction to execute incorrectly if said instruction did not execute incorrectly (Col.15 lines 7-42).

21. Regarding claim 11, Keller has taught the method of claim 10, wherein said dynamically determining said time period comprises shifting said instruction forward for earlier replay if a time slot become available and shifting said instruction backwards for later replay if a resource conflict is detected (see Col.18 lines 1-26). Here, the issue pick circuit selects the oldest eligible instructions from the ROP buffer every clock cycle to be issued/reissued for execution. Because instructions that are to be replayed reside within the ROP buffer, and because the oldest eligible instructions are issued first, every time an instruction is issued out of the buffer, inherently every other instruction is "moved forward" to an earlier time slot in the buffer. Furthermore, because instructions are ineligible for reissuing until their resource conflicts are resolved (see Col.15 lines

33-42), instructions that are to be replayed but still have pending resource conflicts (ineligible instructions) are inherently "moved backwards" into a later time slot in the buffer as they are passed over so younger, eligible instructions can be issued.

22. Regarding claim 12, Keller has taught the method of claim 11, further comprising:

a. Routing said instruction to a delay queue (80 of Fig.4) to wait for said time period to elapse prior to re-executing said instruction if said long latency type of error caused said instruction to execute incorrectly (see Col.15 lines 33-42, Col.17 lines 13-18, Col.18 lines 1-26 and Col.18 line 62 – Col.19 line 7),

b. Routing said instruction from said delay queue (80 of Fig.4) for re-execution after said time period has elapsed (see Col.15 lines 33-42, Col.17 lines 13-18, Col.18 lines 1-26 and Col.18 line 62 – Col.19 line 7).

23. Regarding claim 13, Keller has taught the method of claim 12, wherein said routing of said instruction from said delay queue comprises rescheduling said instruction for re-execution (see Col.18 line 62 – Col.19 line 7).

24. Regarding claim 14, Keller has taught the method of claim 12, wherein said routing of said instruction from said delay queue comprises sending said instruction for re-execution without rescheduling said instruction (see Col.15 lines 33-42, Col.17 lines 13-18, Col.18 lines 1-26 and Col.18 line 62 – Col.19 line 7). Here, when the instruction is actually sent out for re-execution, it is not rescheduled. It does not become rescheduled until it reaches the Scheduler. Thus, the actual routing of the instruction out of the delay queue comprises sending the instruction for re-execution without rescheduling it.

25. Regarding claim 17, Keller has taught a processor comprising:

a. A scheduler (36 of Fig.3) to dispatch instructions (see Col.8 line 51 – Col.9 line 3 and Col.12 lines 24-26),

b. A multiplexer coupled to said scheduler, said multiplexer to receive said instructions from said scheduler (see Col.18 lines 4-16). Here, because a selection is taking place between instructions from the scheduler, and because a multiplexer is defined as selecting between one of a number of inputs and switching its information to the output (see *The Authoritative Dictionary of IEEE Standards Terms*, 7th Ed., p.716), there is inherently a multiplexer performing some sort of multiplexing operation on instructions from the scheduler.

c. An execution unit (40A of Fig.3) coupled to said multiplexer, said execution unit to execute said instructions (see Col.12 lines 24-26),

d. A checker (42 of Fig.3) coupled to said execution unit, said checker to determine whether each instruction has executed correctly (see Col.2 lines 58-66 and Col.15 lines 7-12),

e. A replay mechanism (36 of Fig.3) coupled to said checker (see Fig.3), said replay mechanism to receive from said checker each instruction that has not executed correctly (see Col.20 lines 27-32), said replay mechanism further comprising logic to determine whether a long latency operation caused an incorrectly execution instruction (Col.15 lines 7-42), said logic also to dynamically determine a time period to delay said incorrectly executed instruction if said long latency operation caused said incorrectly execution instruction (see Col.15 lines 33-42 and Col.18 line 62 – Col.19 line 7). Here, the replay mechanism (Scheduler)

already contains the executed instructions, and the checker (load/store unit) further defines to the replay mechanism those instructions that were incorrectly executed and need to be replayed (see Col.20 lines 33-43).

26. Regarding claim 18, Keller has taught the processor of claim 17, wherein said replay mechanism further comprises a delay queue (80 of Fig.4) to store said incorrectly executed instruction (see Col.17 lines 13-18) for said time period prior to releasing said incorrectly executed instruction to said execution unit for re-execution (see Col.15 lines 33-42, Col.18 lines 1-26 and Col.18 line 62 – Col.19 line 7).

27. Regarding claim 25, Keller has taught the processor of claim 17, wherein said replay mechanism comprises an advance/delay queue (80 of Fig.4) to shift said incorrectly executed instruction forward if a time slot opens up and to shift said incorrectly execute instruction backward if a resource conflict is detected (see Col.18 lines 1-26). Here, the issue pick circuit selects the oldest eligible instructions from the ROP buffer every clock cycle to be issued/reissued for execution. Because instructions that are to be replayed reside within the ROP buffer, and because the oldest eligible instructions are issued first, every time an instruction is issued out of the buffer, inherently every other instruction is "moved forward" to an earlier time slot in the buffer. Furthermore, because instructions are ineligible for reissuing until their resource conflicts are resolved (see Col.15 lines 33-42), instructions that are to be replayed but still have pending resource conflicts (ineligible instructions) are inherently "moved backwards" into a later time slot in the buffer as they are passed over so younger, eligible instructions can be issued.

28. Regarding claim 26, Keller has taught a system comprising:

a. A memory (204 of Fig.16) coupled to a bus (202 of Fig.16),

b. A processor (10 of Fig.16) coupled to said bus (see Fig.16), said processor comprising:

I. A scheduler (36 of Fig.3) to dispatch instructions (see Col.8 line 51 – Col.9 line 3 and Col.12 lines 24-26),

II. An execution unit (40A of Fig.3) coupled to said scheduler, said execution unit to execute said instructions (see Col.12 lines 24-26),

III. A first level cache (44 of Fig.1) coupled to said execution unit, said first level cache to store data for said instructions (see Col.9 lines 28-48),

IV. A checker (42 of Fig.3) coupled to said execution unit, said checker to determine whether each instruction has executed correctly (see Col.2 lines 58-66 and Col.15 lines 7-12),

V. A replay mechanism (36 of Fig.3) coupled to said checker (see Fig.3), said replay mechanism to receive from said checker each incorrectly executed instruction (see Col.20 lines 27-32), said replay mechanism further comprising logic to determine whether a long latency operation caused said incorrectly execution instruction (Col.15 lines 7-42), said logic to also dynamically determine a time period to delay said incorrectly executed instruction if said long latency operation caused said incorrectly executed instruction (see Col.15 lines 33-42 and Col.18 line 62 – Col.19 line 7). Here, the replay mechanism (Scheduler) already contains the executed instructions, and the checker (load/store unit) further defines to the replay

mechanism those instructions that were incorrectly executed and need to be replayed (see Col.20 lines 33-43).

29. Regarding claim 27, Keller has taught the processor of claim 26, wherein said replay mechanism comprises an advance/delay queue (80 of Fig.4) to shift said incorrectly executed instruction forward for earlier replay if a time slot opens up and to shift said incorrectly executed instruction backward for later replay if a resource conflict is detected (see Col.18 lines 1-26). Here, the issue pick circuit selects the oldest eligible instructions from the ROP buffer every clock cycle to be issued/reissued for execution. Because instructions that are to be replayed reside within the ROP buffer, and because the oldest eligible instructions are issued first, every time an instruction is issued out of the buffer, inherently every other instruction is "moved forward" to an earlier time slot in the buffer. Furthermore, because instructions are ineligible for reissuing until their resource conflicts are resolved (see Col.15 lines 33-42), instructions that are to be replayed but still have pending resource conflicts (ineligible instructions) are inherently "moved backwards" into a later time slot in the buffer as they are passed over so younger, eligible instructions can be issued.

30. Regarding claim 28, Keller has taught the system of claim 26, wherein said replay mechanism further comprises a delay queue (80 of Fig.4) to store said incorrectly executed instruction for said time period (see Col.17 lines 13-18), said delay queue to release said incorrectly executed instruction to said execution unit for re-execution after said time period has elapsed (see Col.15 lines 33-42, Col.18 lines 1-26 and Col.18 line 62 – Col.19 line 7).

31. Regarding claim 29, Keller has taught the system of claim 28, further comprising a retirement unit (32 of Fig.1) coupled to said checker, said retirement unit to retire each instruction receive from said checker that executed correctly (see Col.8 lines 26-42).

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claims 5 and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Keller et al., U.S. Patent No. 6,622,235 as applied to claims 1-4 and 17-18 above, respectively, and further in view of Akkary et al., U.S. Patent No. 6,182,210.

34. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in

accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

35. Regarding claim 5, Keller has taught the method of claim 4, but has not explicitly taught wherein the method further comprises tracking the number of times said instruction is executed and re-executed.

36. However, Akkary has taught the use of a replay counter to track the number of times an instruction is replayed so that the correct replay iteration of the instruction can be identified when more than one iteration is in the pipeline concurrently, allowing the correct results to be written into the appropriate data arrays (see Col.11 lines 9-16, Col.22 lines 45-60 and Col.23 line 1-12). One of ordinary skill in the art would have recognized that it is desirable to have a processor execute instructions correctly and provide correct results. Therefore, one of ordinary skill in the art would have found it obvious to modify the method of Keller to further include a counter to track the number of times an instruction is replayed so that the processor computes the correct results when more than one replay iteration of an instruction is in the pipeline at the same time.

37. Regarding claim 19, Keller has taught the processor of claim 18, but has not explicitly taught wherein said replay mechanism further comprises a counter to count a number of times said incorrectly executed instruction is executed and re-executed.

38. However, Akkary has taught the use of a replay counter to track the number of times an instruction is replayed so that the correct replay iteration of the instruction can be identified when more than one iteration is in the pipeline concurrently, allowing the correct results to be written into the appropriate data arrays (see Akkary, Col.11 lines 9-16, Col.22 lines 45-60 and Col.23 line 1-12). One of ordinary skill in the art would have recognized that it is desirable to have a processor execute instructions correctly and provide correct results. Therefore, one of ordinary skill in the art would have found it obvious to modify the method of Keller to further include a counter to track the number of times an instruction is replayed so that the processor computes the correct results when more than one replay iteration of an instruction is in the pipeline at the same time.

Allowable Subject Matter

39. Claims 6-8, 15-16, 20-24 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. While the method of "exponential backoff", comprising tracking of the number of times an operation fails in a counter and increasing the retry delay if the counter value increases and decreasing the delay if the counter value decreases, has been taught by the prior art of record (see Hughes et al., and Herlihy), and further the prior art of record has taught the use of a replay counter to keep track of the number of times an instruction as been replayed (see Akkary et al.), the method has not been applied to instruction replay systems such that the replay delay is varied based upon the replay counter value, as claimed in claims 6, 15, 20 and 30, and thus there is no motivation to combine the teachings with

prior art of record applied above (Keller et al.). Furthermore, claims 7-8, 16 and 21-24 are also objected to for being dependent on objected parent claims, although the limitations in claims 7-8, 16 and 21-24 have been taught in the prior art of record and are well known.

Conclusion

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

41. Herlihy, U.S. Patent No. 5,553,627, has taught a method that uses a counter to keep track of the number of failed attempts to access a shared memory resource, and increases the delay between attempts as the counter value increases.

42. Hughes et al., U.S. Patent No. 6,427,193, has taught a method for implementing exponential backoff to increase the delay between failed memory operation attempts as the number of failed attempts increases, thus avoiding deadlock situations.

43. Merchant et al., U.S. Patent No. 6,094,717, has taught an instruction replay system with multiple delay queues that detects whether an incorrect execution was the result of a long latency operation.

44. Leibholz et al., U.S. Patent No. 6,098,166, has taught a method for reissuing instructions that executed incorrectly.

45. Merchant et al., U.S. Patent No. 6,163,838, has taught an instruction replay system with multiple delay queues that detects whether an incorrect execution was the result of a long latency operation.

46. Merchant et al., U.S. Patent No. 6,665,792, has taught an instruction replay system with multiple delay queues that detects whether an incorrect execution was the result of a long latency operation.

47. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

48. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

RICHARD L. ELLIS
PRIMARY EXAMINER

BJO
7/21/2004